Low-Power Analog Processing with RF Correlation for Ultra-High Speed Receivers: Unlocking the ADC

techUK Workshop on: 6G Software Defined Radio and RF Sampling

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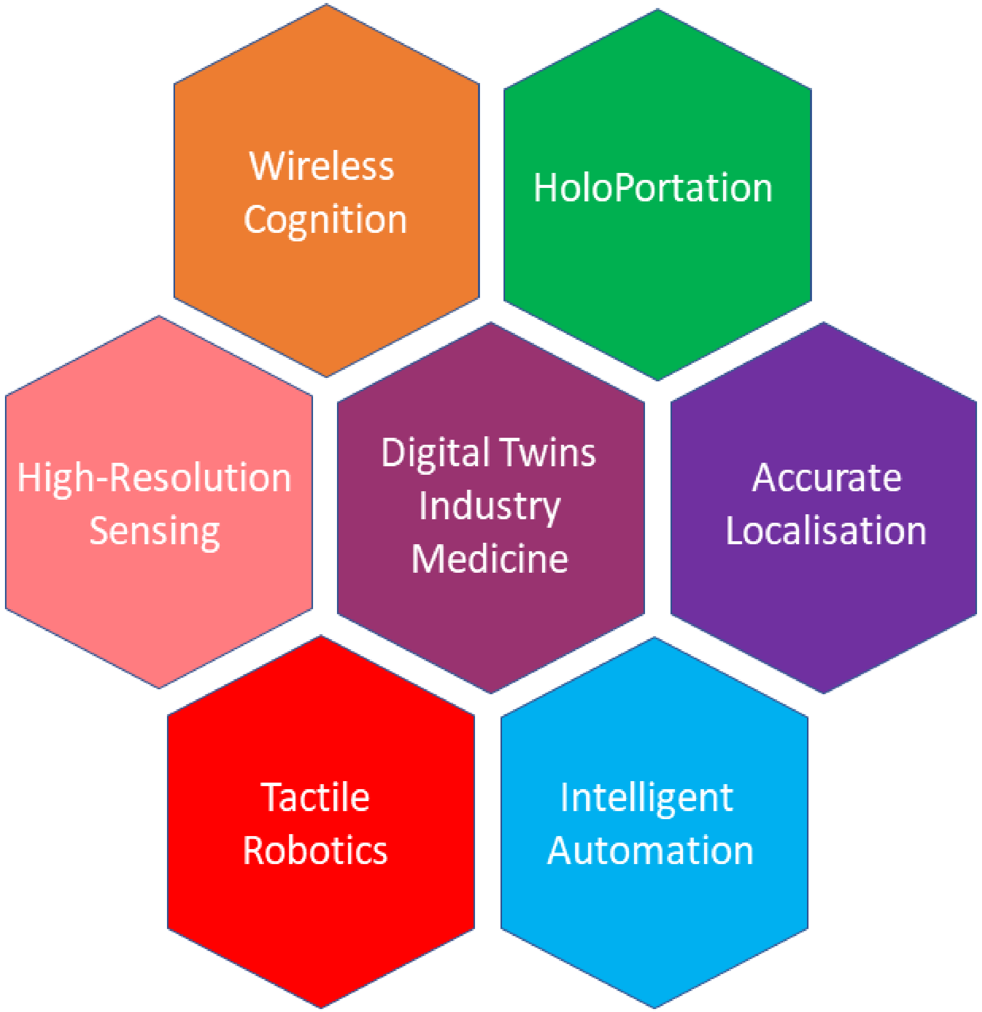
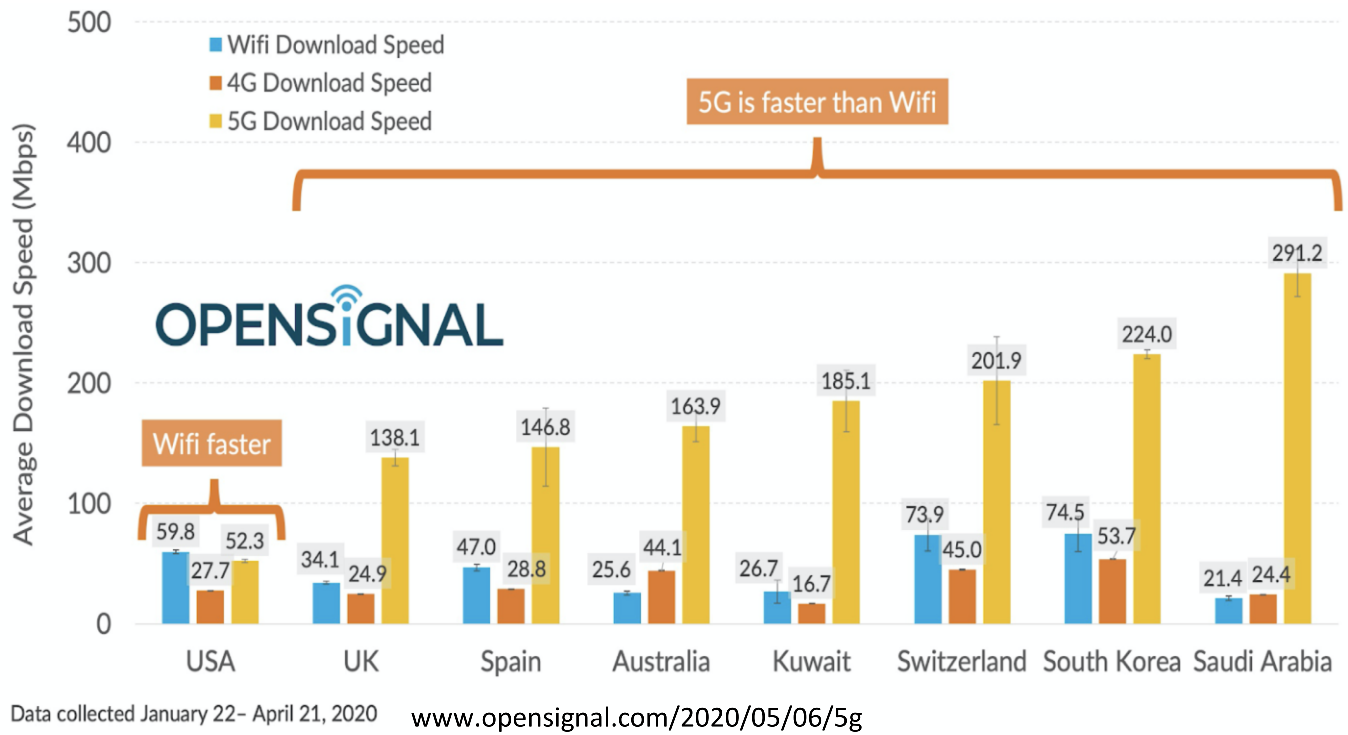
BACKGROUND



- Exponential growth of advanced technologies such as artificial intelligence (AI), robotics, internet-of things (IoT), virtual/augmented reality (VR/AR), and automation is ushering in unprecedented paradigm shifts in wireless communication.
- Vision is termed by the International Telecommunication Union (ITU) as Network 2030 networks in 2030 and beyond capable extremely fast response in critical situations and meeting high-precision communication demands of emerging market verticals.



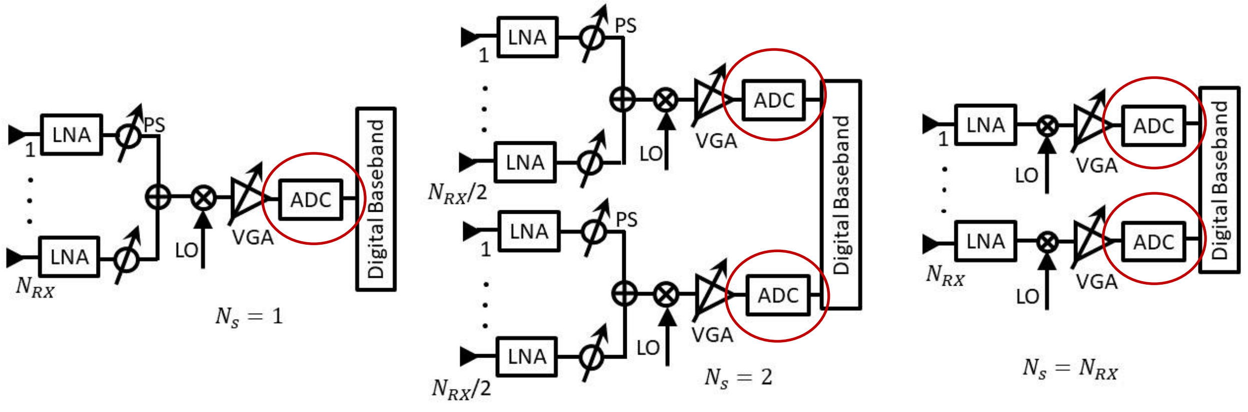
www.opensignal.com/2020/05/06/5g

- ➢ To realise such a vision networks will require ultra-high speed (UHS) data rates of 1 terabit per second (Tb/s). That is more than 100 times faster than 5G networks, with ultra-low latency as well as very high precision in information timing.
- ➢ Following commercialization of 5G technologies, current trends are now for initiating research activities to shape the communication networks beyond 5G (B5G); i.e. towards Network 2030 and beyond.

CURRENT APPROACH

- Analog BF, Hybrid BF and Digital BF
- All require ADCs

Initial work on Massive MIMO

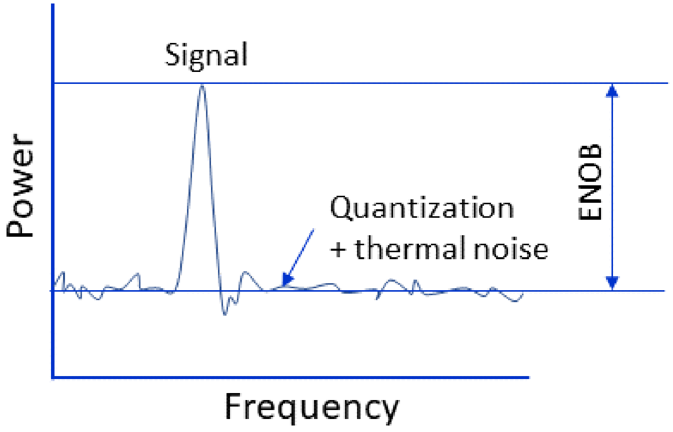


Analog BF   Hybrid BF   Digital BF

Can be employed; Low resolution PS, sparse channels, codebook design.

High angular resolution; Low bit ADCs

ADC



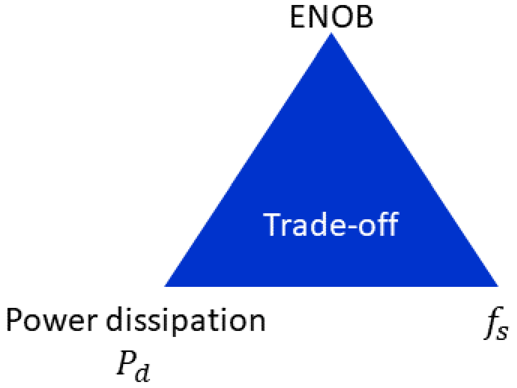


Figure-of merit $FOM_{ADc} = P_d/(f_s 2^{ENOB})$ [1]

ADC ENERGY EFFICIENCY

Thermal sampling noise $N_s = kT/C_s$ where:
C_s is the sampling capacitor of the ADC
k Boltzmann's Constant
T temperature in Kelvin

Normally it is ensured that $N_s \sim N_q$ for which [2]:

$$C_s = 12kT2^{2n}/(V_{in}^2)$$

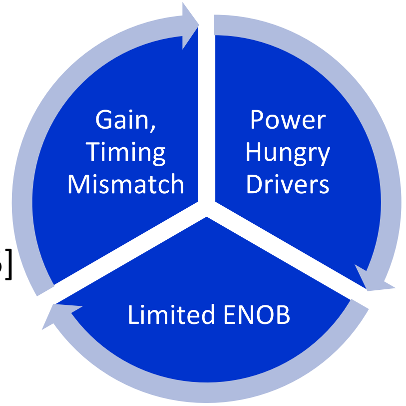
where V_{in} is the full-scale voltage at ADC input and ENOB= $n - 0.5$

High resolution ADC ($n > 10$) $P_d \propto 2^{2n}$ (thermal noise)
Low resolution ADC ($n < 10$) $P_d \propto 2^{n}$ (capacitor mismatch/size)
Technology/Lower voltage values → Lower noise permissible levels → Larger capacitor size→ P_d again dominated by thermal noise.

ADC HIGH SPEED RESOLUTION

At high speed a minimum resolution is required across bandwidth.
Due to parasitic capacitances ADC power and speed become nonlinear lowering the FOM.
ADC operating beyond certain FOM have degrading performance on speed and resolution.

Possible solution:
Time interleaved ADCs

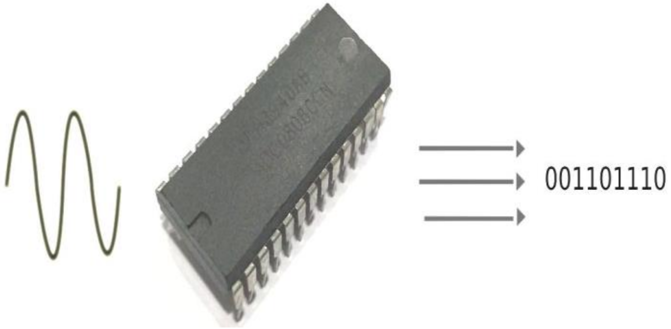


[3]-[5]

High Power
~930 mW

[5]

ADC



At Tb/s you are beyond what technology can achieve.

- Poor resolution
- Power inefficiency

Current state of the art CMOS technology does enable circuits to generate signals up to 1.3 THz. **But ADCs with this technology will require high power, almost ~2-3W!.** For mobile phone currently~0.1-0.5 W. Current devices employ oscilloscopes.

Teledyne Oscilloscope
~ 6Kg

DIRECT DEMODULATION WITHOUT ADC

OOK
BPSK
QPSK
~16 Gb/s
[6]-[8]

8 PSK
Challenging due to reduced boundary regions

8 PSK
Implemented by employing look-up tables.
High latency [9]

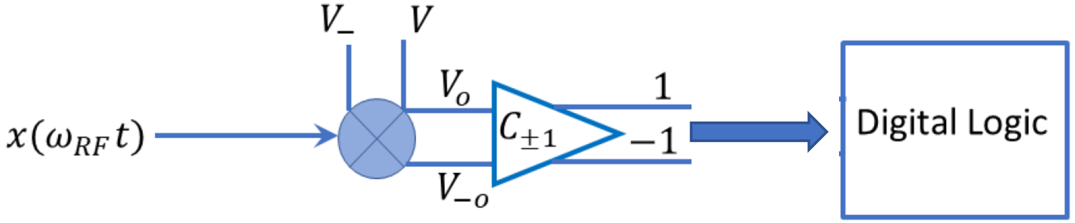
8 PSK
Overcomes latency by employing RF correlation
Limited to 8 PSK [10]

Fixed modulation architectures, not reconfigurable

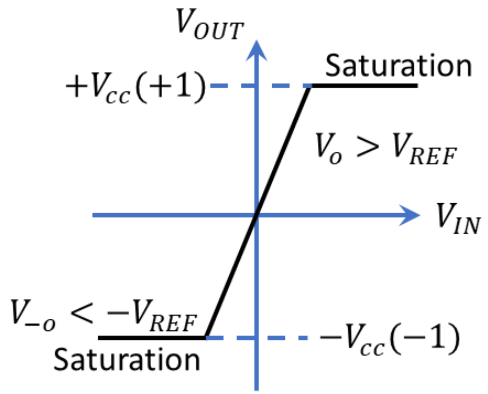
BPSK, QPSK/4-QAM, 16-QAM
Low power analog processing with RF correlation

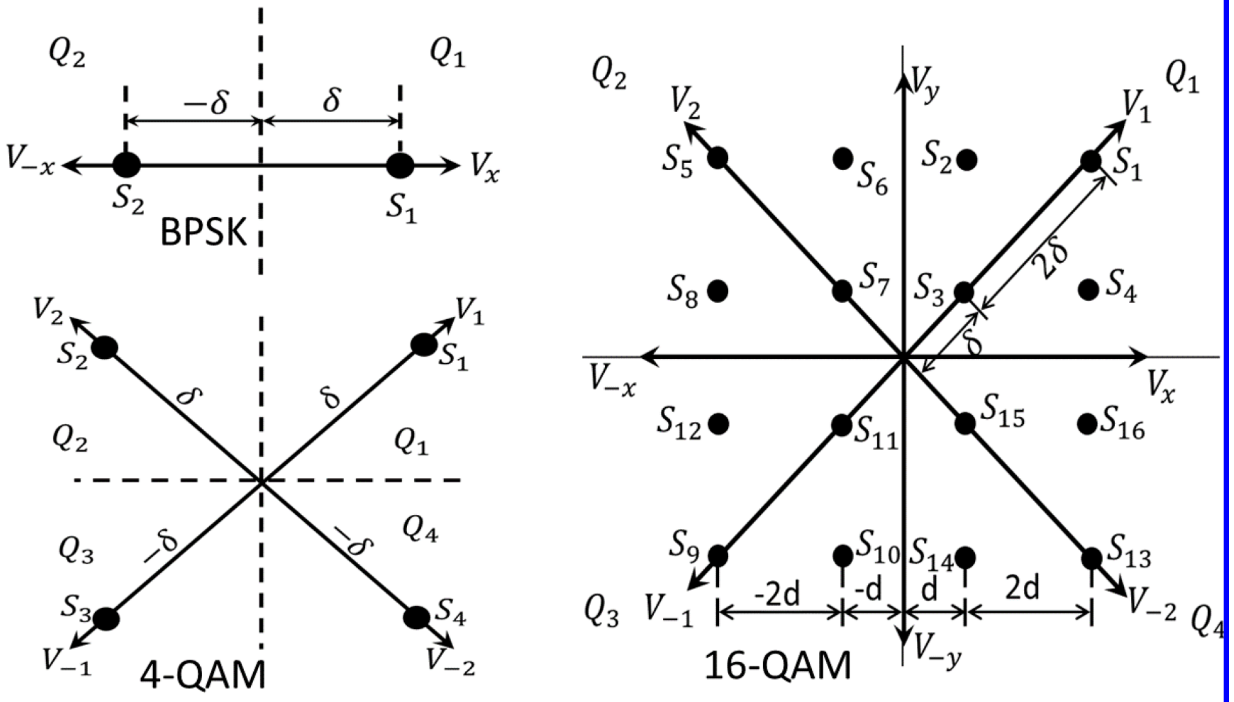
- Reconfigurable
- Highest for 16 QAM reported so far

LOW POWER ANALOG PROCESSING (LPAP)
WITH RF CORRELATION



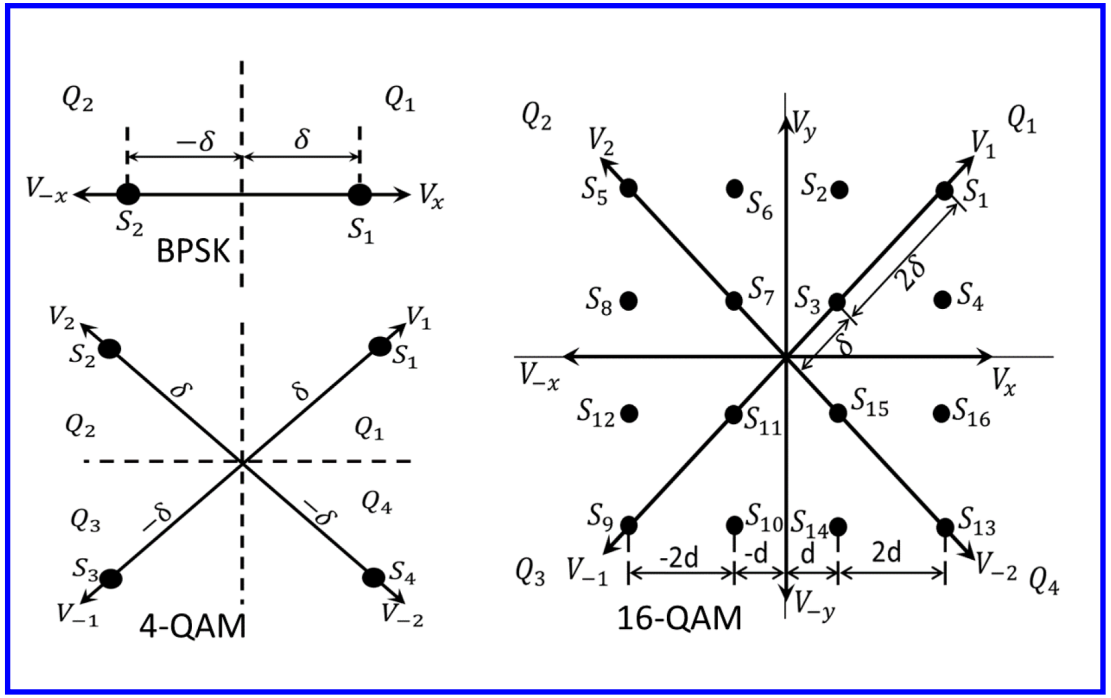
$$V_{o\pm} = \frac{1}{T_s}\int_{-T_s2}^{T_s2} x(\omega_{RF}t)V_{\pm}dt$$

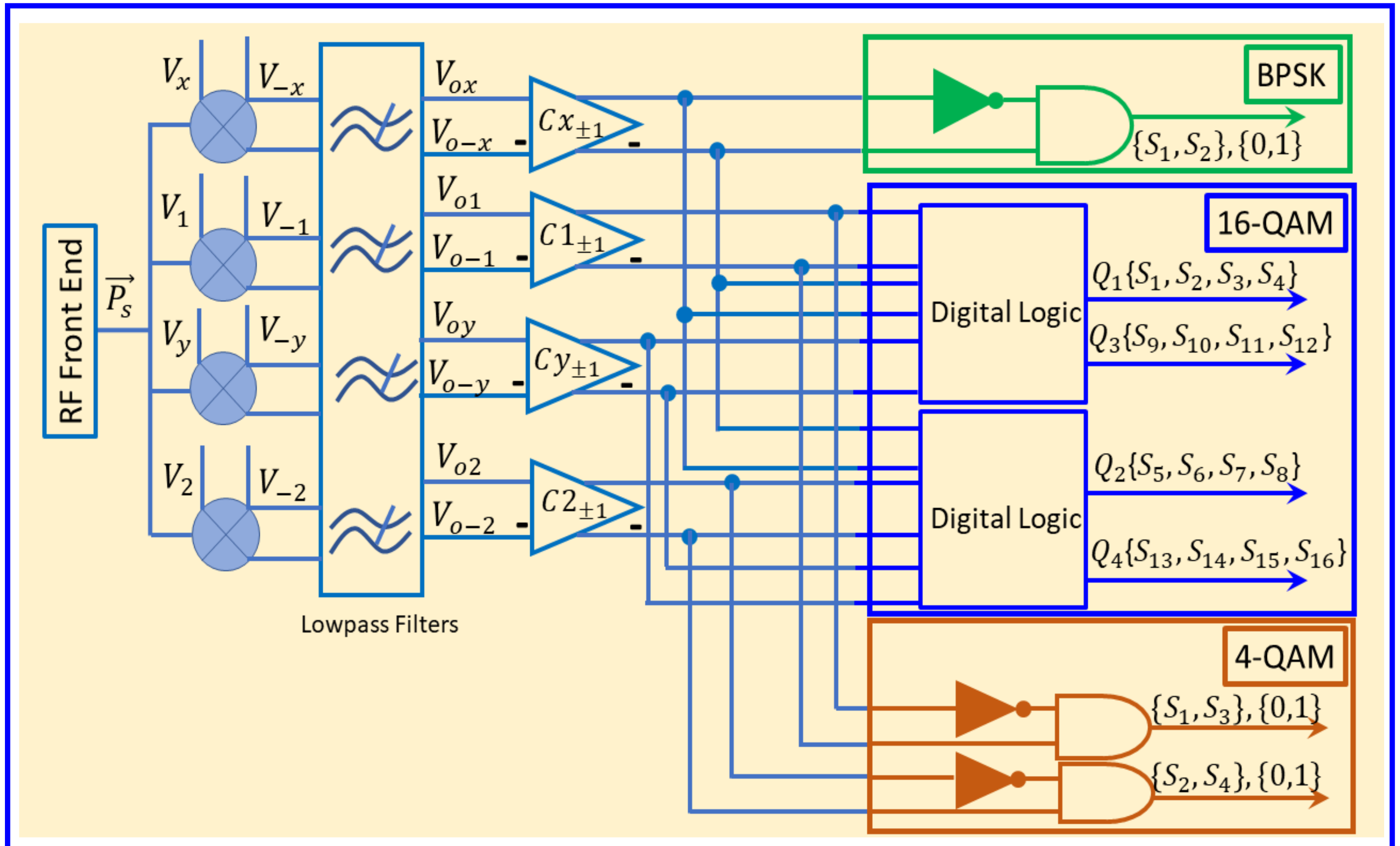




Modulation	LO	Phase
BPSK	$V_{\pm x}$	$[0^o, 180^o]$
4-QAM	$V_{\pm 1}$, $V_{\pm 2}$	$[45^o, 225^o]$, $[135^o, 315^o]$
16-QAM	$V_{\pm x}$, $V_{\pm 1}$, V, $V_{\pm 2}$	$[0^o, 180^o]$, $[45^o, 225^o]$, $[90^o, 270^o]$, $[135^o, 315^o]$

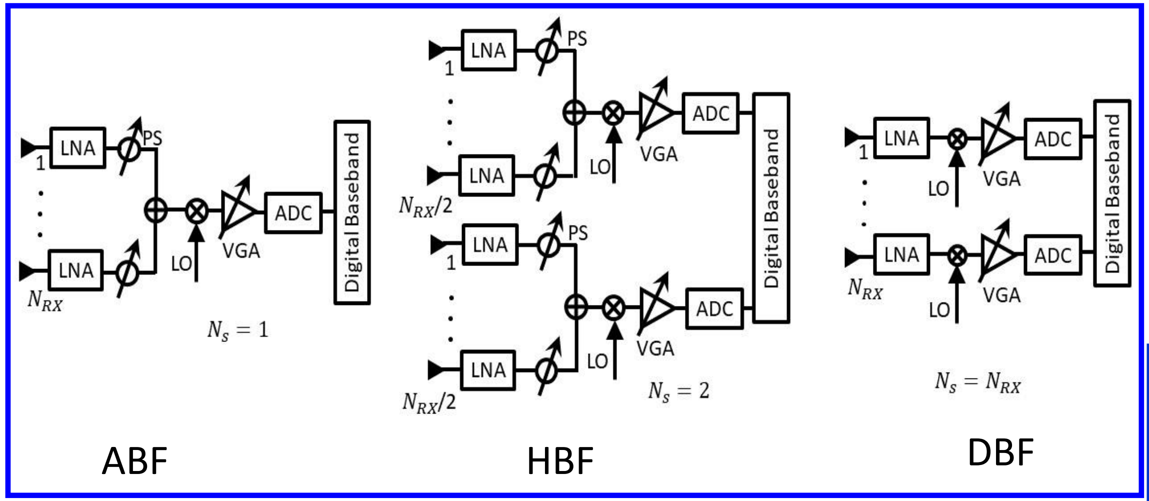
LPAP ARCHITECTURE

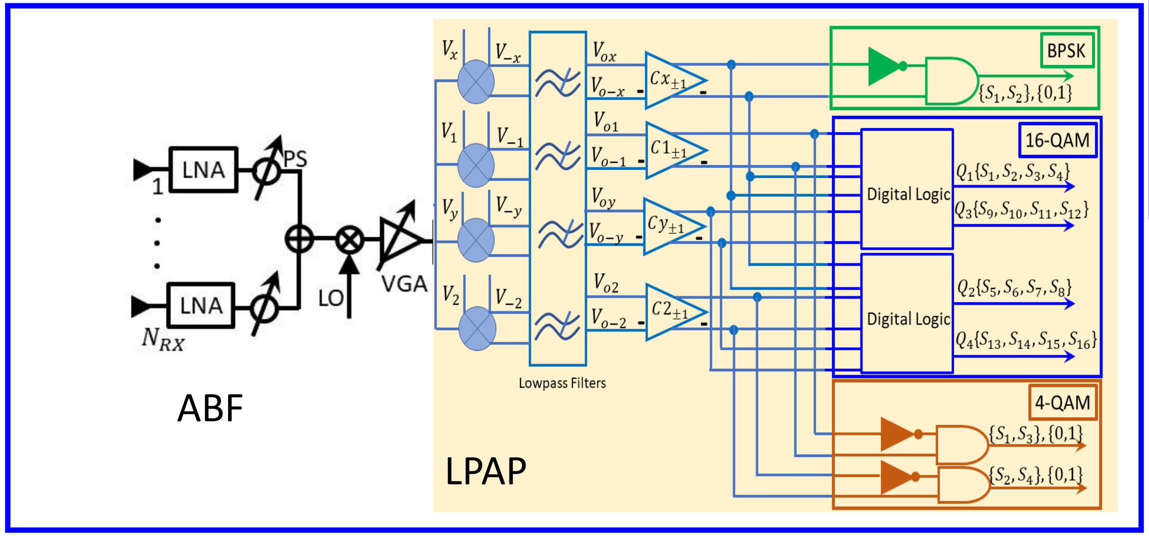




Single architecture multiple modulations: BPSK, 4-QAM, 16-QAM

POWER CONSUMPTION





AFE includes all components between antenna and ADC which include LNA, PS and VGA.

PS, mixers, LOs are considered to be passive devices that introduce insertion loss but do not draw any power ... taken [A] ... phase shifters, L_{PS} is 10 dB [11]. L of mixer is 6 dB and power drawn by the mixer from the LO is 10 dBm [12].

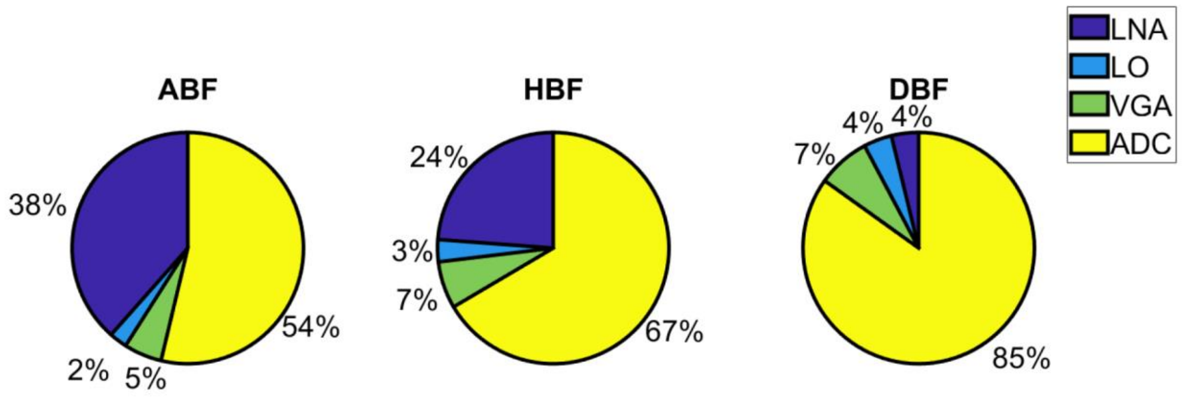
The state of art ADC in 20 nm CMOS has a FOM of 0.24 pJ and has sampling rate of 16 GS/s with ENOB 6 bits [5]. Using FOM we determine the power consumed by the ADC.

LPAP requires additional mixers and LOs along with comparators, with numbers varying depending on modulation type i.e. BPSK, 4- or 16-QAM. VGA ensures adequate signal power to drive the following Rx stages. There are no ADCs.

- For ABF and HBF ...
- $N_s = 1$ for ABF and 2 for HBF
- For DBF $N_s = N_{RX}$

Receiver	Power Consumption [mW]					
BF	LNA	LO	VGA	ADC	Comparator	Total
ABF	153.99	10	21.26	215.00	-	400.25
HBF	153.99	20	42.52	430.00	-	646.51
DBF	153.99	160	297.81	3440.00	-	4051.80
LPAP	[redacted]					
BPSK	153.99	20	21.26	-	2	197.25
4-QAM	153.99	30	21.26	-	4	209.25
16-QAM	153.99	50	21.26	-	8	233.25

POWER CONSUMPTION



LOW RESOLUTION ADC (ENOB 3.5-4)

- Modest sample rates ~ 1GS/s
- Require additional algorithms for synchronisation, user scheduling and beamforming.

LOW RESOLUTION ADC (ENOB 3.5-4)

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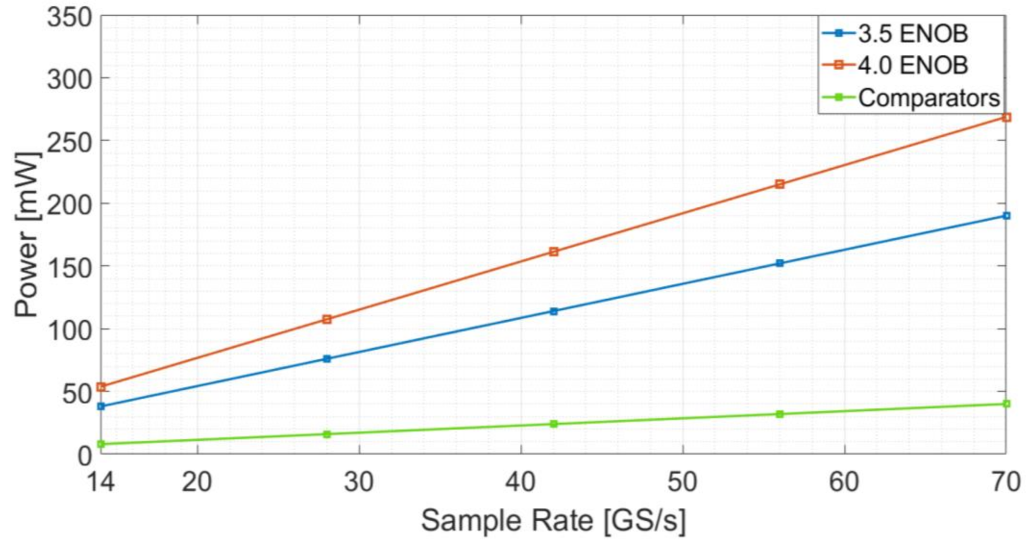

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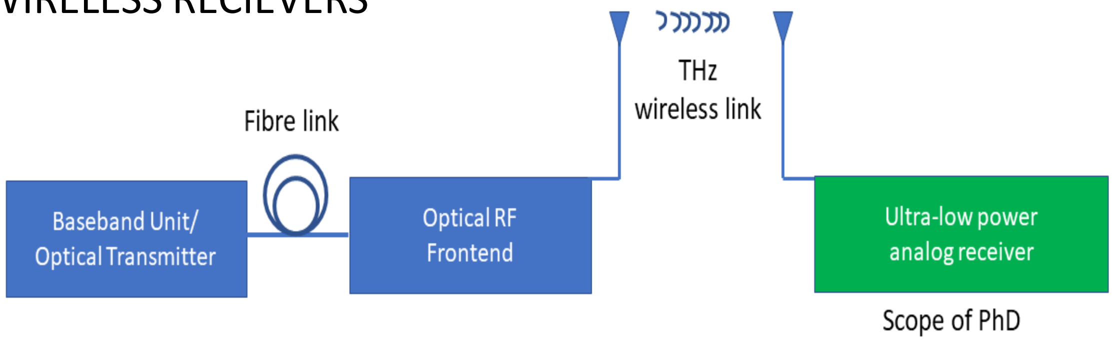
UNLOCKING THE FIBRE WITH LOW-POWER ULTRA-HIGH SPEED WIRELESS RECIEVERS



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- Low-power transmitters, receivers circumventing the use of power-hungry ADCs, DACs.
- Ultra-wideband amplifiers.
- Passive or active sub-THz and THz circuits
- Integrated hybrid electronic-photonic transmitters, compound semiconductor receivers.
- Low-power baseband processing for ultra-low latency and very-high throughput.
- Other challenges such as high precision in information timing.

THANK YOU

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