StrathSDR
University of Strathclyde Software Defined Radio

RF Sampling and Software Defined Radio:
Working with a 4GHz Baseband using the Multichannel RFSoC

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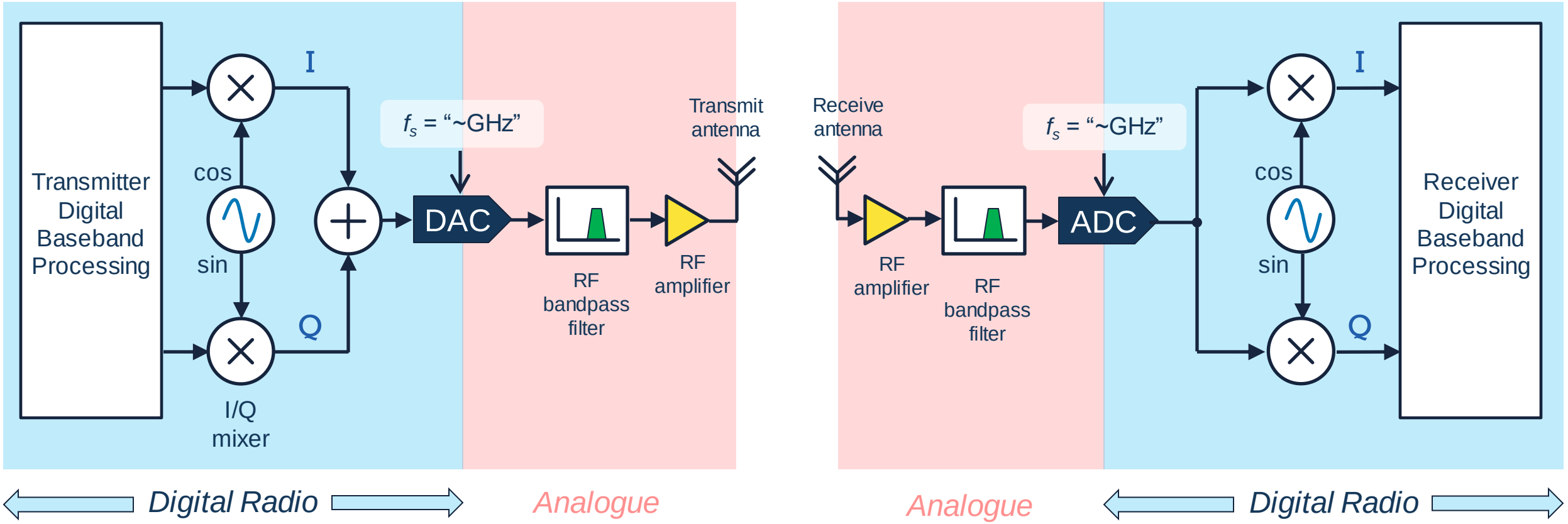
https://sdr.eee.strath.ac.uk

Outline

StrathSDR

- (Almost) all digital radio
- RF sampling review – GHz samplers
- RFSoC architecture and features
- Xilinx partnership RFSoC toolflow R&D programme
- Software Defined Radio (SDR) toolflow
- Live SDR demonstration: single chip spectrum analyser, f_s = 4GHz
- Available open source materials and further support
- (What's next – 5G OpenRAN SDR!)

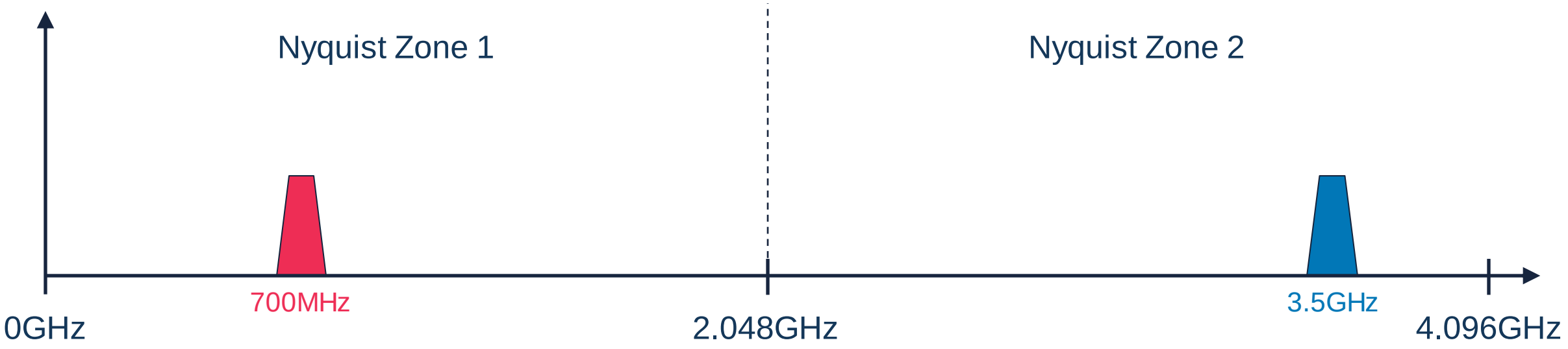
(Almost) All Digital Radio Architecture



- With ADCs and DACs that operate at multi-GHz sampling rates, the analogue / digital interface can be at RF frequencies.
- Almost all radio functionality is implemented digitally.

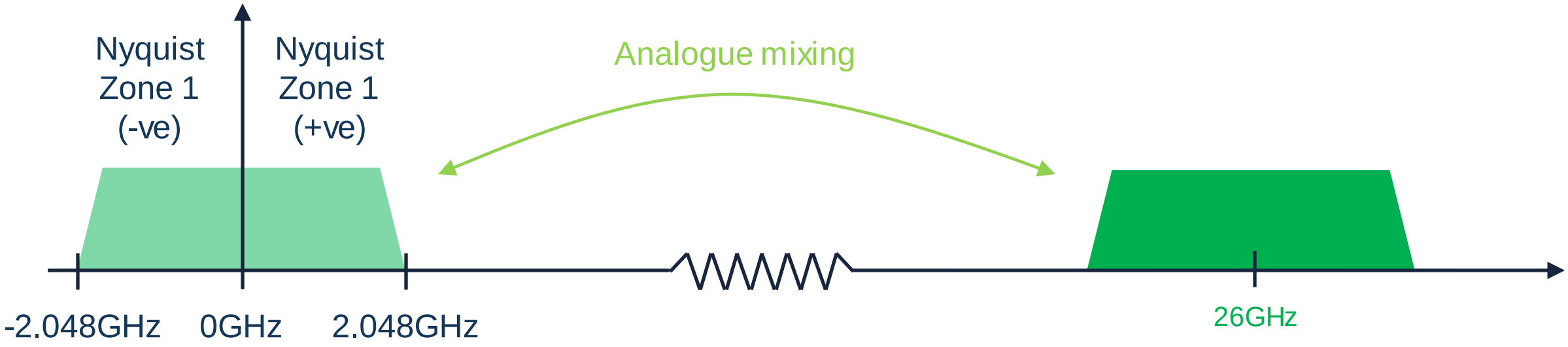
RF Sampling and Nyquist Zones

- ADCs and DACs can operate at multiple GHz sampling rates (here we assume f_s = 4.096GHz).
- Some 5G and 6G bands can be directly digitised, using either the first or second Nyquist Zone.
- For instance, bands at 700MHz and 3.5GHz can be supported in Zones 1 and 2 as shown below.



Higher Frequency Bands

- Higher frequencies (> 4.096GHz) can be accommodated using an external (analogue) mixing stage, with the ADC and DAC operating at complex baseband.
- In this configuration, a signal bandwidth approaching 4GHz can be handled using a pair of RF-DACs / RF-ADCs.
- Potential for 6G applications in high frequency bands.



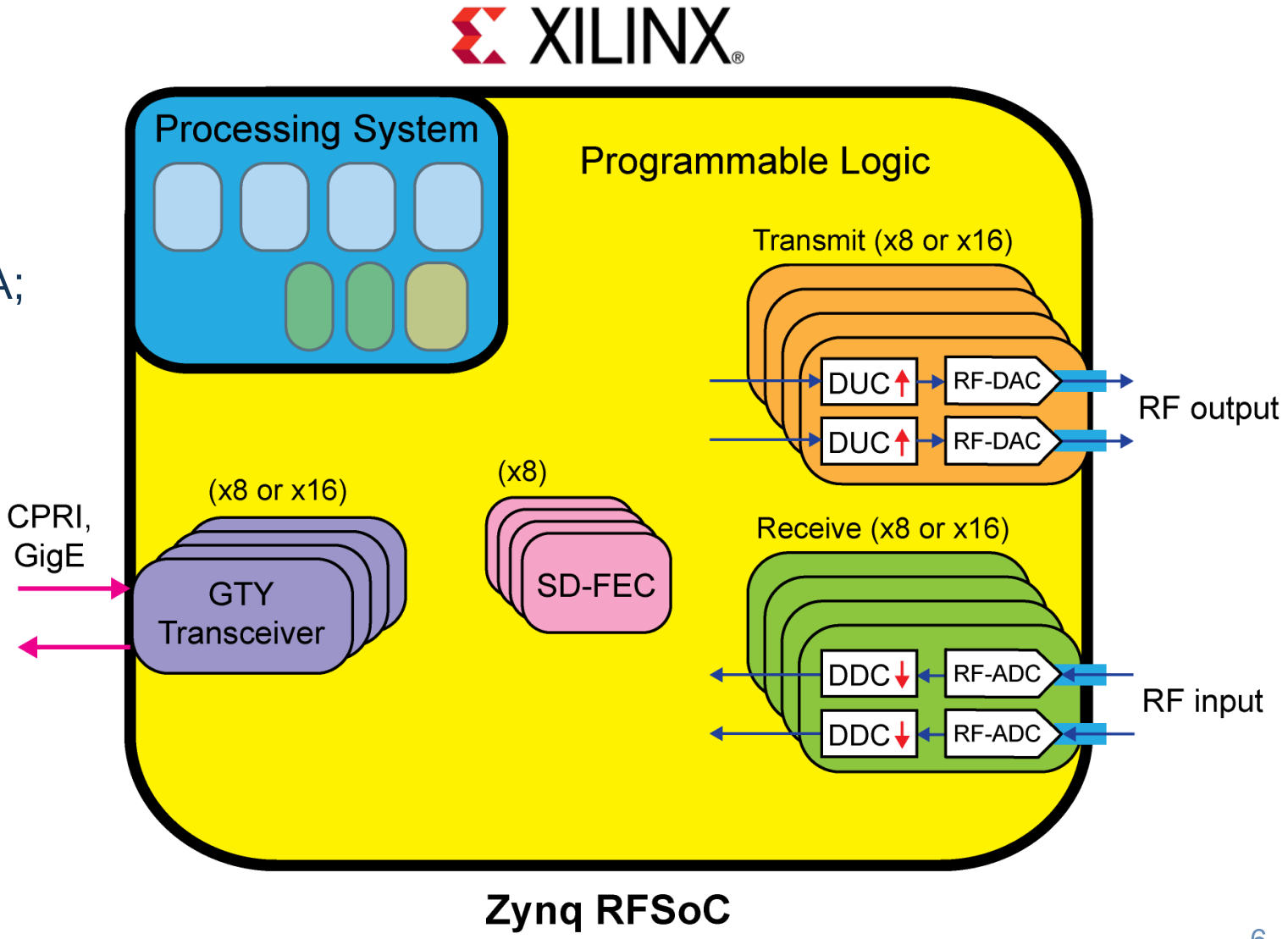
Xilinx Radio Frequency System on Chip (RFSoC)

The RFSoC integrates:

- **RF-DACs** and **RF-ADCs**: high rate RF data converters (multi-GHz);
- **Programmable Logic**, i.e. an FPGA;
- A **Processing System** with 4 applications and 2 real-time processor cores;
- Soft Decision Forward Error Correction (**SD-FEC**) blocks;
- High speed **transceivers** for wired connections

… all on **a single chip**.

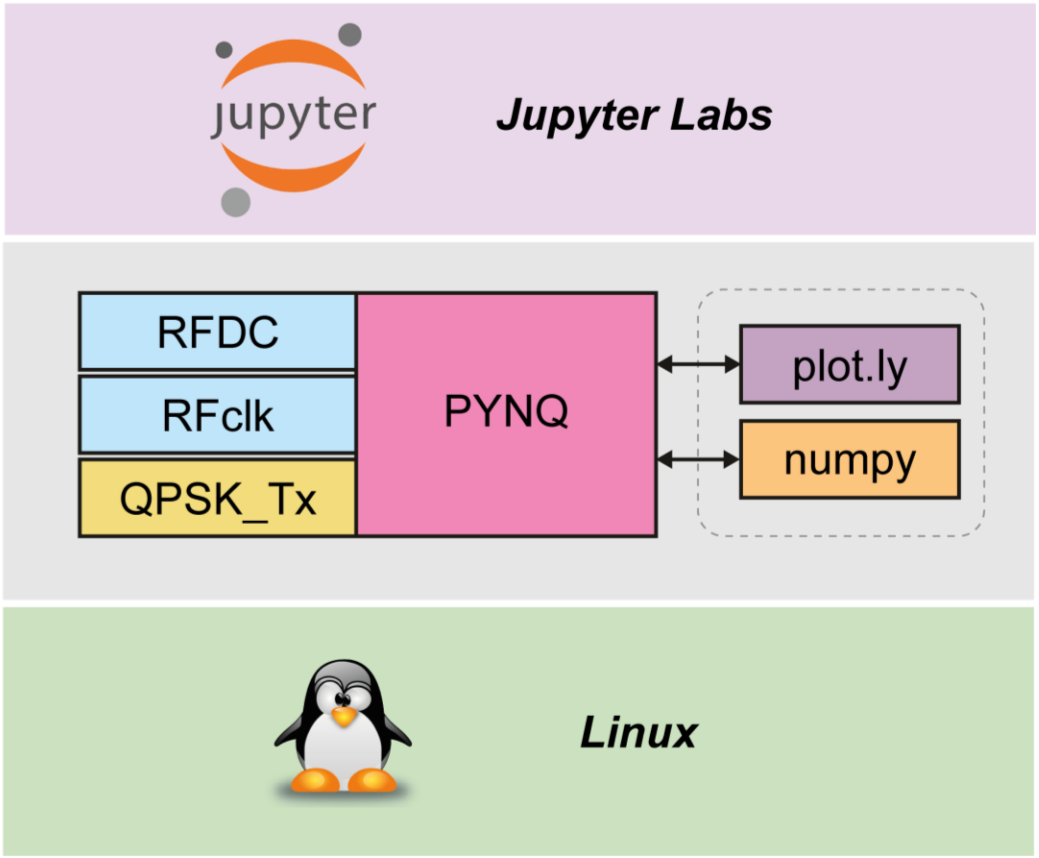
- Widely used by Tier1s and Tier2s



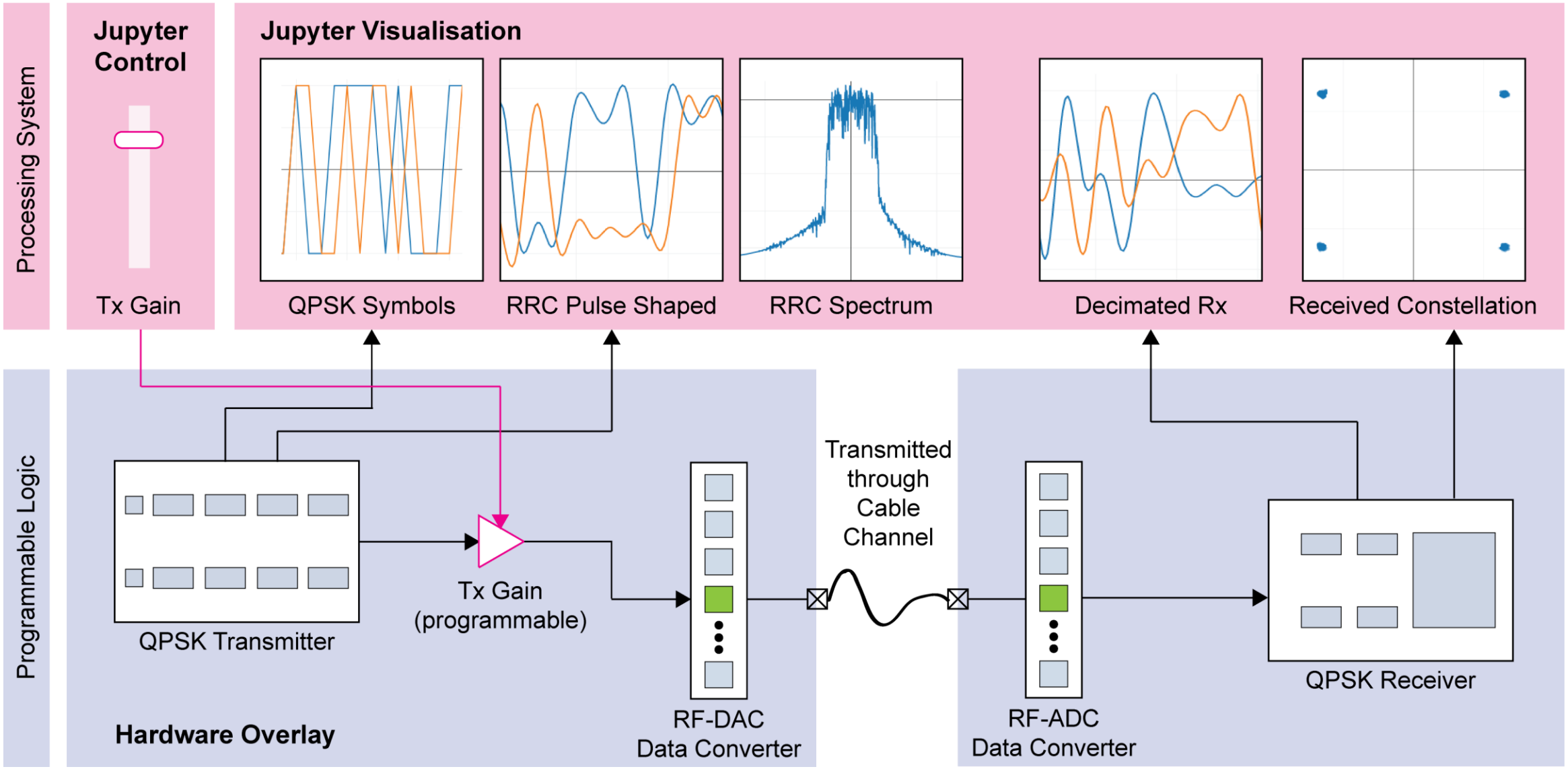
RFSoC / SDR Toolflow Research

- Building RFSoC systems is a relatively complex design task.
- In partnership with Xilinx, Strathclyde research focuses on toolflows for SDR development, based around the ***PYNQ software framework.***
- PYNQ provides a ***Python-based*** user interface for controlling aspects of software and hardware functionality, and introspection.
- Created PHY layer DSP/SDR design flow for next generation, spectrum agile radio.

PYNQ Block Diagram (Tx example)

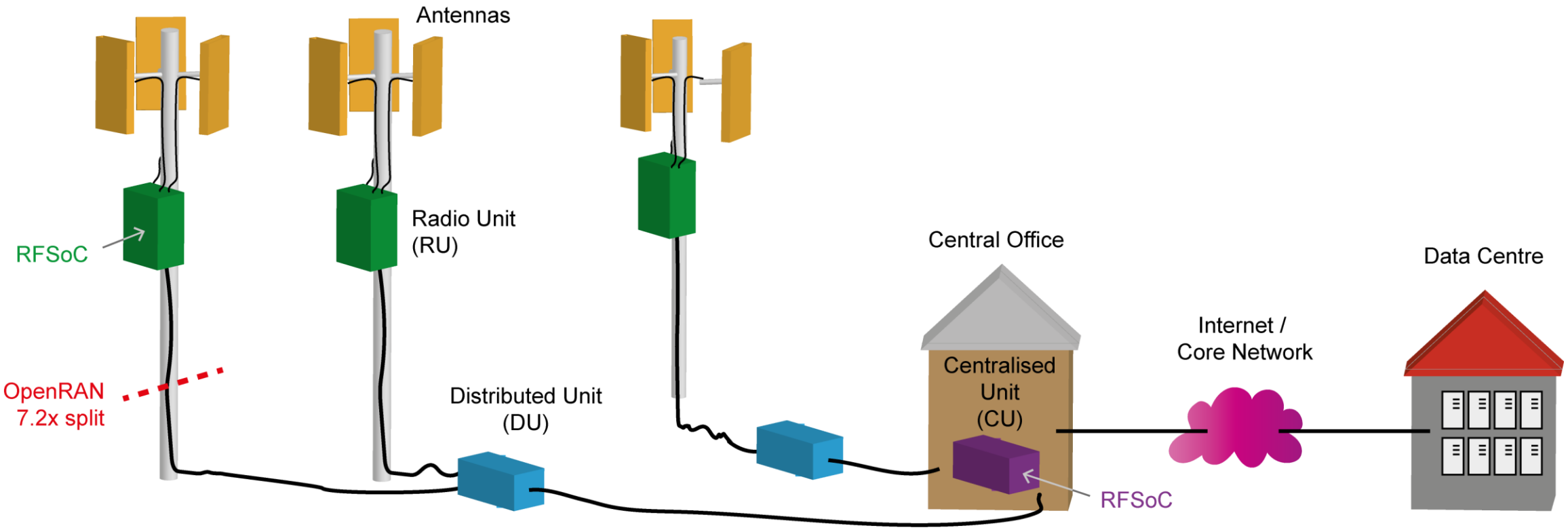


Simple Reference Design: QPSK



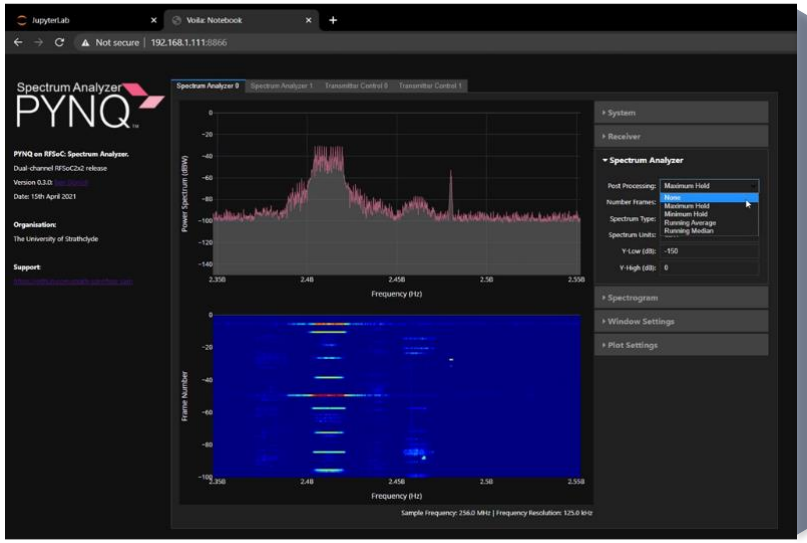
SDR Opportunities

- This integrated platform is a real, desktop and spectrum agile SDR system.
- RFSoC is currently being used in 5G gNodeBs, both in the Radio Unit and in centralised functions (e.g. using SD-FEC blocks).
- Technology is still developing (larger bandwidths, lower power, more integration…).

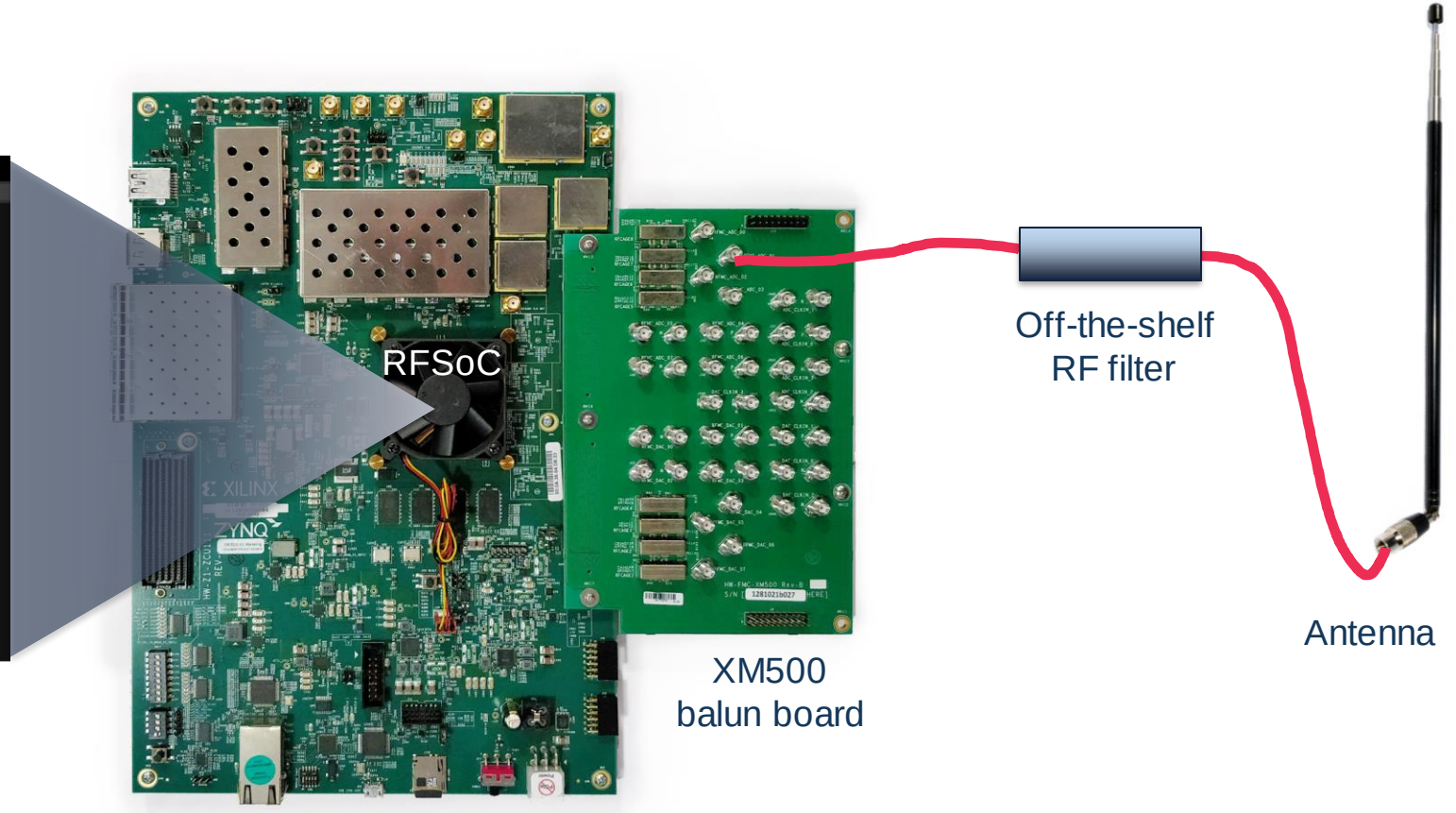


Demo: RFSoC Single-Chip Spectrum Analyser

- We will now present a live demonstration of a single chip spectrum analyser application, developed using RFSoC and the PYNQ SDR design flow.

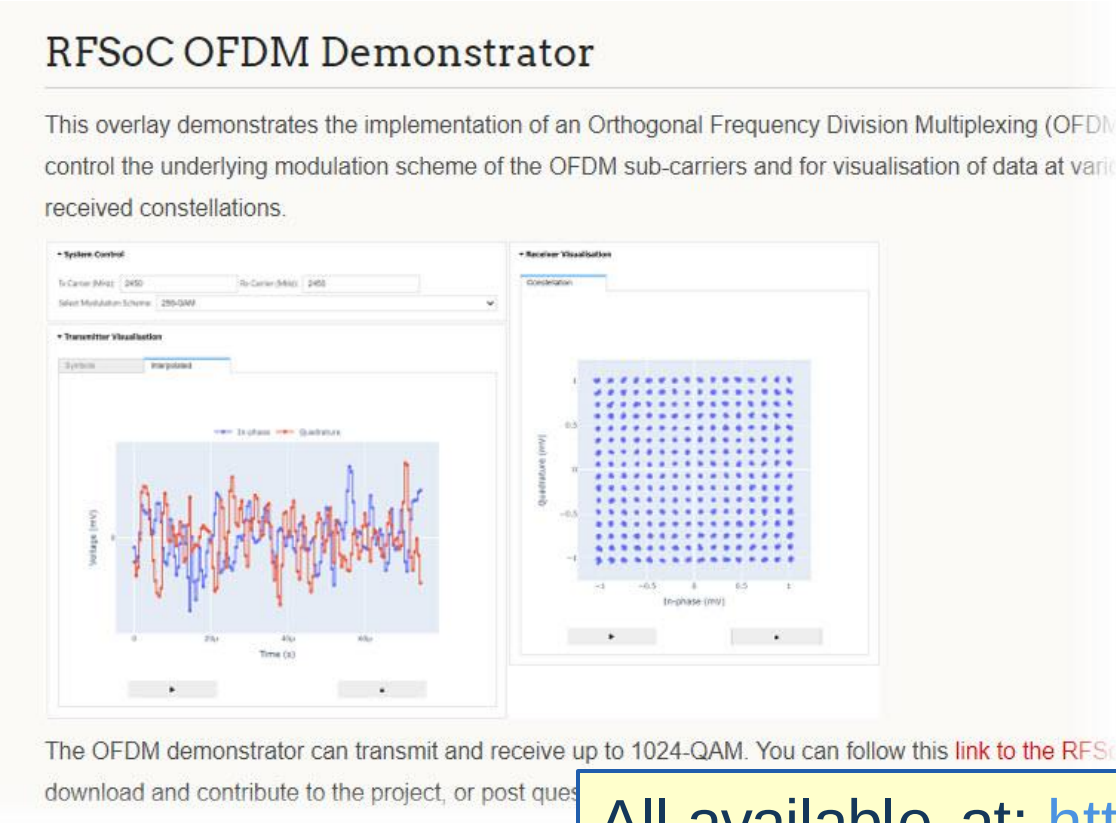


PYNQ Spectrum Analyser
(running on the RFSoC chip, accessed via standard web browser)

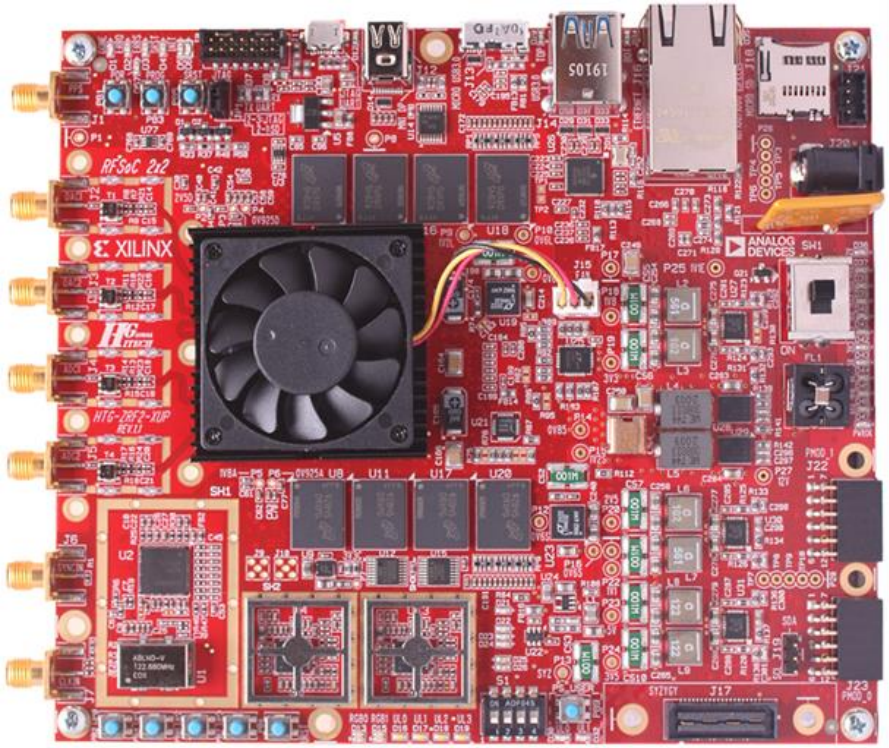


Open Source Materials and Further Support

- Strathclyde has created an accessible set of **open source** materials (demos, tutorials, notebooks) suitable for new users.



- Xilinx offers a low-cost development board for academia – the **RFSoC 2x2** – which is available for Univs to purchase by application.



All available at: http://www.rfsoc-pynq.io/

Acknowledgements

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  - Liam Madden (San Jose) — Executive Vice President, *and* General Manager, Wired and Wireless Group
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Thank You.

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